What is claimed is:

1. A semiconductor device comprising:

an NMOS transistor and a PMOS transistor each formed on a substrate, channel regions of the NMOS transistor and the PMOS transistor comprising strained silicon,

wherein a gate of the NMOS transistor has work function that exceeds a work function of a gate of the PMOS transistor so as to compensate for a difference in respective threshold voltages of the NMOS transistor and the PMOS transistor caused by the strained silicon channel regions.

2. The device claimed in claim 1, wherein the difference in the work functions of the NMOS and PMOS gates is approximately the same as the difference in the threshold voltages of the NMOS and PMOS transistors.

3. The device claimed in claim 1, wherein the gate of the NMOS transistor is fully silicided and the gate of the PMOS transistor is partially silicided.

4. The device claimed in claim 3, wherein the fully silicided NMOS gate and the partially silicided PMOS gate comprise nickel.

5. The device claimed in claim 1, wherein the substrate is a semiconductor substrate.

6. The device claimed in claim 1, wherein the substrate is a silicon on insulator (SOI) substrate

7. The device claimed in claim 6, wherein the NMOS transistor and PMOS transistor are FinFETs.

8. The device claimed in claim 1, wherein the NMOS transistor and the PMOS transistor comprise a CMOS device.

9. A method of forming a semiconductor device, comprising:

forming an NMOS transistor and a PMOS transistor having respective gates each comprising a polysilicon portion and a silicide portion, wherein channel regions of the NMOS transistor and the PMOS transistor comprise strained silicon;

forming a metal layer in contact with the silicide portion of the NMOS gate while protecting the PMOS gate; and

annealing to fully silicide the NMOS gate.

10. The method claimed in claim 9, wherein, after annealing, the gate of the NMOS transistor has a work function that exceeds a work function of the gate of the PMOS transistor so as to compensate for a difference in respective threshold voltages of the NMOS transistor and the PMOS transistor caused by the strained silicon of the channel regions.

11. The method claimed in claim 10, wherein the difference of the work functions of the NMOS and PMOS gates is approximately the same as the difference of the threshold voltages of the NMOS and PMOS transistors.

12. The method claimed in claim 9, wherein forming a metal layer in contact with the silicide portion of the NMOS gate while protecting the PMOS gate comprises:

forming a conformal protective layer over the NMOS transistor and the PMOS transistor;

forming a silicon oxide layer over the protective layer;

planarizing the silicon oxide layer to exposed portions of the protective layer above the respective gates;

masking the PMOS transistor;

etching the protective layer to expose the silicide portion of the NMOS gate; and

forming the metal layer in contact with the exposed silicide portion of the NMOS gate.

13. A method of forming a semiconductor device, comprising:

forming an NMOS transistor and a PMOS transistor having respective polysilicon gates, wherein channel regions of the NMOS transistor and the PMOS transistor comprise strained silicon;

removing a portion of the NMOS gate;

forming a metal layer in contact with the NMOS gate and the PMOS gate; and

annealing to form a fully silicided NMOS gate and a partially silicided PMOS gate.

14. The method claimed in claim 13, wherein, after annealing, the gate of the NMOS transistor has a work function that exceeds a work function of the gate of the PMOS transistor so as to compensate for a difference in respective threshold voltages of the NMOS transistor and the PMOS transistor caused by the strained silicon of the NMOS channel region.

15. The method claimed in claim 14, wherein the difference of the work functions of the NMOS and PMOS gates is approximately the same as the difference of the threshold voltages of the NMOS and PMOS transistors.

16. The method claimed in claim 13, wherein removing a portion of the NMOS gate comprises:

forming a conformal protective layer over the NMOS transistor and the PMOS transistor;

forming a silicon oxide layer over the protective layer;

planarizing the silicon oxide layer to expose portions of the protective layer above the respective gates;

masking the PMOS transistor;

etching the protective layer to expose the NMOS gate; and

etching to remove a portion of the NMOS gate.

17. The method claimed in claim 16, wherein forming a metal layer in contact with the NMOS gate and the PMOS gate is preceded by etching the protective layer to expose the PMOS gate.

18. A method of forming a semiconductor device, comprising:

forming an NMOS transistor and a PMOS transistor having respective polysilicon gates, wherein channel regions of the NMOS transistor and the PMOS transistor comprise strained silicon;

partially siliciding the PMOS gate while protecting the NMOS gate; and

fully siliciding the NMOS gate while protecting the PMOS gate.

19. The method claimed in claim 18, wherein, after forming said partially silicided PMOS gate and the fully silicided NMOS gate, the gate of the NMOS transistor has a work function that exceeds a work function of the gate of the PMOS transistor to compensate for a difference in respective threshold voltages of the NMOS transistor and the PMOS transistor caused by the strained silicon of the NMOS channel region.

20. The method claimed in claim 19, wherein the difference of the work functions of the NMOS and PMOS gates is approximately the same as the difference of the threshold voltages of the NMOS and PMOS transistors.

21. The method claimed in claim 18, wherein selectively forming a fully silicided NMOS gate while protecting the PMOS gate comprises:

forming a conformal protective layer over the NMOS transistor and the PMOS transistor;

forming a silicon oxide layer over the protective layer;

planarizing the silicon oxide layer to expose portions of the protective layer above the respective gates;

masking the PMOS transistor;

etching the protective layer to expose the NMOS gate;

forming a metal layer in contact with the NMOS gate; and

annealing to form the silicide portion of the NMOS gate.

22. The method claimed in claim 21, wherein forming the metal layer is preceded by etching to remove a portion of the polysilicon NMOS gate.